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Precision Manufacturing Using Advanced Optical Interference Lithography

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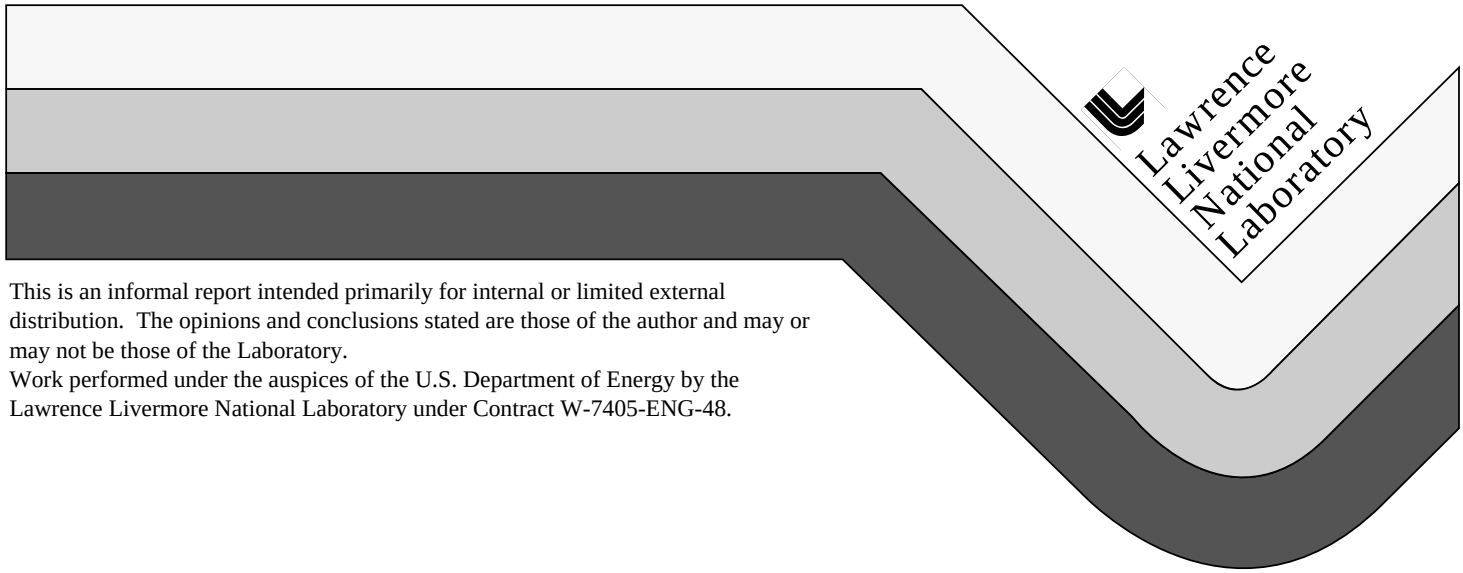

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FINAL REPORT
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Summary

The primary goal of this LDRD project was to develop interference lithography (IL) as a reliable process for patterning large-area, deep-submicron scale field emission arrays for field emission display (FED) applications. We have developed a system based on IL which can easily produce an array of 0.2 to 0.5 micron emitters over large area (up to 400 sq. in demonstrated to date) with better than 5% height and spacing uniformity. Process development as a result of this LDRD project represents a significant advance over the current state of the art for FED manufacturing and is applicable to the fabrication of all types of FEDs, independent of the emitter material.

The ability of IL to pattern such structures simultaneously and uniformly on a large format has application in other industries of strategic importance to U.S. high-technology, such as dynamic random access memory (DRAM) production, and magnetic media recording. The following pages describe the economic potential of FED's, their operating characteristics, and how IL has been demonstrated to be a superior method for their fabrication. Following this are brief descriptions of other preliminary work we have done in applying IL to DRAM and magnetic structure patterning.

Field Emission Flat Panel Displays

Flat panel displays (FPD's) currently represent an $8 billion per year market projected to grow to over $20 billion by the end of the decade.[1] This market is overwhelmingly dominated by active matrix liquid crystal displays (AMLCDs). AMLCD technology is controlled almost solely by the Japanese with a US market share of less than 3%.[2] To address this market imbalance, the US government formed the United States Display Consortium (USDC) and assembled a White House Flat Panel Display Task Force, chaired by Kenneth Flamm. One of the important conclusions to emerge from both USDC studies and the White House task force was that to develop a viable domestic supplier of flat panel displays, US firms could either partner with an established Japanese manufacturer of AMLCDs such as Sharp or "leapfrog" AMLCD technology with a new approach. Three such technologies have emerged: plasma, electroluminescence and field emission.

A plasma display panel (PDP) consists of two glass substrates, each containing an array of electrodes. The substrates are separated by approximately 100 microns. When between 100 and 200 volts is applied across the electrodes comprising a pixel, the fill gas between the plates (typically neon) undergoes avalanche breakdown and emits line radiation characteristic of the fill gas. PDPs are well suited to large-area monochrome displays operating at the red line of neon. Color PDPs are under development and there has been significant progress in color PDPs this past year. Nevertheless, PDPs have significant limitations:

1) the light output of a pixel is determined by the number of gas atoms excited, hence, the brightness of a pixel is determined by its area.

2) light is radiated isotropically from the discharge resulting in crosstalk between pixels

3) the cost of manufacture is approximately twice that of AMLCDs.

4) the large power consumption of PDPs makes them unsuitable for portable display applications

Electroluminescent displays (EL) rely on the electrical breakdown of a phosphor dot. ELs are attractive in niche markets because of their high brightness and wide-angle viewability. They are not expected to impact the consumer market due to difficulties in obtaining efficient blue phosphors resulting in limited color range and expensive cost of manufacture.

Field emission displays (FEDs) are composed of an array of submicron cathodes which emit electrons via tunneling. These electrons are accelerated

across a vacuum gap and impinge on a phosphor-coated screen to emit light (figure 1). Each pixel acts as a microscopic cathode ray tube (CRT). Instead of a single electron beam sweeping across an array of phosphor pixels as in a conventional CRT, the field emission display is comprised of millions of individual CRTs. In order to function with low voltage (5-10 volts), all FEDs require submicron cathodes in order to produce the enormous field strengths ($\approx 10^7$ V/cm) necessary to establish tunneling through the surface barrier of the cathode material.[3,4] Since the current grows exponentially with applied voltage, direct x-y addressing of the cathode matrix can be achieved without the need for a transistor at each pixel. As a result, groups of emitters can be addressed in parallel providing inherent redundancy. FEDs produce high brightness over the full range of color with low power consumption. Indeed, to quote a recent *Information Display* report, "Field emission display technology is an extremely exciting and promising FPD technology, which could have a substantial impact on the world FPD market if the manufacturing hurdles can be overcome."[5] When compared directly to current AMLCDs, FEDs are potentially superior performers in all significant categories (Table I).

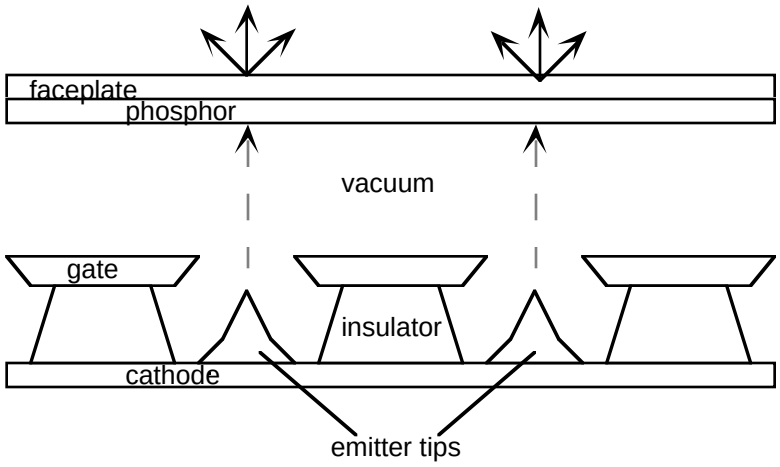

Figure 1: Field emission display concept (from ref. 2).

The main problem with FEDs is that fabrication requires expensive and complex micromachining technology. The field-emitter tips are extremely small -- < 100 atoms wide- and must be made uniformly over the entire screen area.[6] Specifically, commercialization of FEDs is limited by the manufacturing problem of how to cost effectively fabricate a large periodic array of sub-micron emitter structures.

Table I: Performance comparison of field emission displays and AMLCDs (from ref.4)*

	FED (projected)	**AMLCD**
Thickness	6-10 mm	23 mm
Weight	<0.20 kg	0.33 kg
Contrast ratio	>100:1	60:1 to 100:1
Viewing angle	>80°	±45° H, ±30° V
Maximum Brightness	>200 Cd/m^2	60 Cd/m^2
Power Consumption at 60 Cd/m^2	< 1Watt	4 Watts
Operating Temperature	-50 to 80° C	0 to 50° C
Large format capability	Yes	Not likely due to yield and cost

*Based on a typical 5 x 7.5 in notebook size display

Interference Lithography for FED Patterning

It is this manufacturing problem that was addressed by this LDRD project. The requirements for an FED are demanding: a regular array of 0.2-0.5 micron emitters uniform to within 5% over the full area of the display. Such patterns could be produced only up to a few sq. inches with even the most advanced state of the art lithographic techniques. Electron beam lithography is capable of producing the required patterning on small formats. Unfortunately, e-beam lithography is prohibitively expensive in production and does not scale to large area. However, because the emitters are arranged in a regular array, they could in principle be produced by an altogether different approach: interference lithography.

Interference lithography, also known as holographic lithography, has been used in a variety of applications for over fifteen years.[7] The technique is based on the pattern produced by two interfering laser beams of wavelength, λ. The standing wave, sinusoidally varying interference pattern produces alternating light and dark fringes with a spacing, d, determined by the angle at which the beams intersect, θ, according to $d=\lambda/2\sin\theta$. When photoresist is exposed to this pattern and subsequently developed, a surface corrugation is produced whose spacing may be as small as $\lambda/2$. For a typical near ultraviolet or violet laser operating in the range 0.35 - 0.45 microns, lines down to 0.2 microns can be fabricated. By multiple exposures, essentially any pattern which can be formed by intersecting lines (lines, grids, triangles, dots) can be fabricated by this technique.

The ability to make regular linear surface features has led to the use of laser interference lithography for fabricating diffraction gratings. This "holographic" grating production is by far the widest application of interference lithography. Such gratings are typically produced by overcoating the sinusoidal surface relief pattern produced in the exposed and developed photoresist with a thin metal film.[8] Master holographic gratings are available commercially at sizes up to 100 sq. in..[9]

In order to apply interference lithography to the manufacture of large scale (>1000 sq. in.) arrays, we had to developed specialized techniques to address the problems of photoresist coating, uniformity and precision of the critical dimension, depth of field, etc. Our lithography system utilizes a number of new techniques, including meniscus coating of photoresist,[10] and in situ monitoring of the developing grating pattern.[11] The majority of these techniques have been developed as part of the Petawatt LDRD and Laser Programs project, as part of an effort to produce meter-scale submicron-pitch diffraction gratings for pulse compression of a Nova laser beam.

The adaptation of our process developed for large-area grating patterning to large-area field emission patterning was straightforward. By exposing the photoresist coated substrate two times with a 90^{o} rotation in between, and interpreting the in-situ development monitoring signal differently, we were able to achieve two-dimensional patterns. The major area of development required for useful emitter array patterning was in optimizing the photoresist properties to meet the requirements of downstream emitter processing. After patterning, the emitter array undergoes a variety of processing steps including reactive ion etching, metal and insulator deposition, and thermal processing. The exact processing sequence is unique to every manufacturer, but in general the patterned photoresist feature, which defines the critical dimension of the final emitter tip, must be sharply defined with a near-vertical sidewall, and be of a precise width with respect to the spacing between the emitters. Each had additional requirements as to feature height, sidewall angle, areal uniformity, and substrate reflectivity as well. During the course of this work we have characterized a variety of photoresists, and have optimized processing steps so as to make vertical-sidewall resist features with more than 4:1 height-to-width aspect ratio, and duty cycles (ratio of feature width to feature period) ranging from 0.2 to 0.5.[12,13] Examples of these types of patterns are shown in figure 2.

Having integrated these fabrication technologies and optimized photoresist processing, we asked for and received actual FED substrates from several U.S. display producers and lithography vendors to validate our exposure process for actual display fabrication. Some of these corporations have successfully converted the resist pattern of figure 2 into functioning

emitter arrays. An example of a display substrate patterned by LLNL, produced by FED Corp., is shown in figure 3. The display demonstrated a reduction by a factor of seven in the turn-on voltage compared with displays produced by conventional lithographic processes.

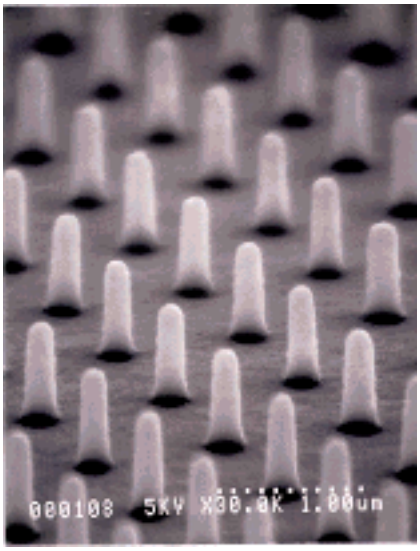

Figure 2: Field emitter post pattern mask made with large format IL. The posts have a base width of <0.25 µm and a height over 0.6 µm.

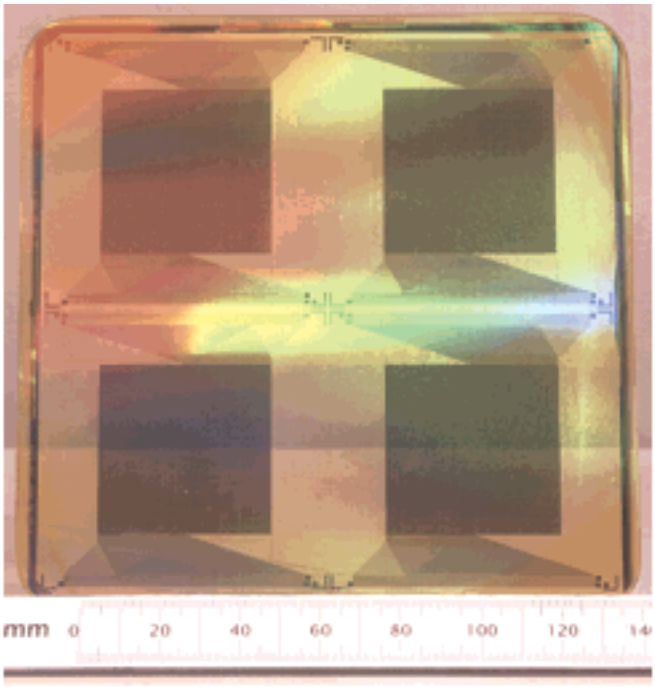

Figure 3: Display plate produced by FED Corp. and patterned by LLNL IL system.

Other manufacturers desire a hole pattern instead of a post pattern. Our process is equally robust at producing a hole pattern as shown in figure 4. This pattern contains 0.25 µm holes on 0.67 µm centers. From this hole pattern, field emitters are easily produced using a standard Spindt evaporation process. A final example is the production of caps in a mask/evaporation process as shown in figure 5.

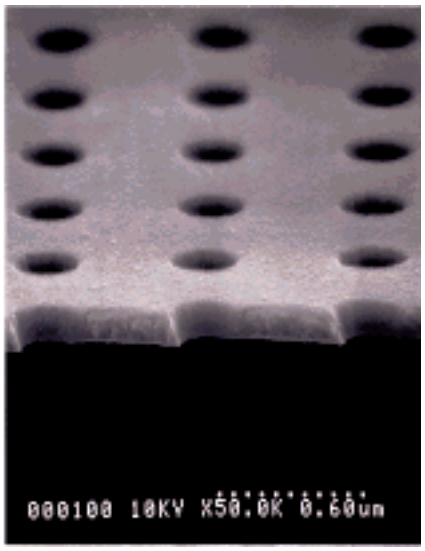

Figure 4: Field emitter mask formed of holes instead of posts.

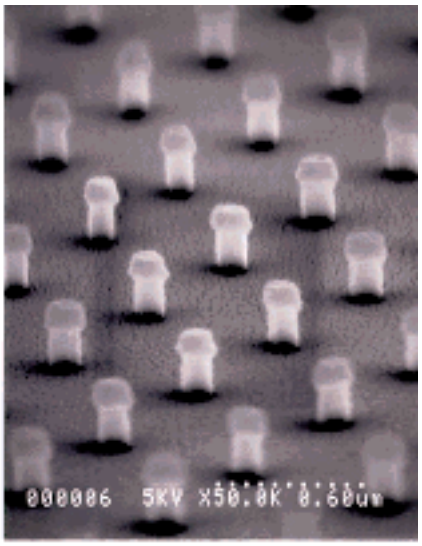

Figure 5: Field emitter mask of capped posts.

Each of the patterns shown in figures 2, 4, and 5 are routinely fabricated on large format in a single exposure. Although the examples shown here were emitter masks on a 0.67 µm spacing, essentially any emitter density can be achieved by simply changing the angle at which the beams interfere. We have produced arrays with a spacing as small as 0.5 µm (400 million emitters/cm^2) and as large as 3 µm (>10 million emitters/cm^2). As a result of the extreme periodicity of the array, cross talk (shorting) between emitters is easily controlled.

LLNL researchers garnered an R&D100 award in 1996 entitled 'Lithography for Flat Panel Displays' as a result of this work. Key to the award were strong letters of recommendation from FEDCorp and Motorola, two of the companies for which patterning experiments were carried out. R&D 100 awards go to developments which are of great potential impact to U.S. industry, and the award is recognition of the significant commercial application of this technology.

Other Applications of Interference Lithography

Laser interference lithography will find direct use in other applications where 0.2 to 100 micron rectilinear (lines, grids, dots) patterns are required. Although there are numerous examples, the most significant other near term application of our system may be a new method for the lithography step in DRAM (dynamic random access memory) manufacture. DRAMs require multiple arrays of submicron structures, which are well suited to interference lithography. DRAM manufacture represents a current $80 B per year market. Due to time and resource constraints, we have made only preliminary investigations into the use of IL for patterning DRAM features. We have patterned rectangular arrays of test structures with minimum feature sizes of 0.15 μm onto 2 in. Si wafers. The density and shape of these test patterns were consistent with the projected requirements for a 1 Gbit DRAM.

We have also used IL to pattern single domain magnetic structures for high density magnetic recording applications[14]. Arrays of cobalt dots with diameters of 100 nm and densities of $>7x10^9/in^2$ have been patterned on silicon substrates by exposing and developing holes in photoresist as described in previous sections, thermally evaporating cobalt onto the Si exposed, and subsequently lifting off the remaining photoresist layer. Using magnetic force microscopy, we have shown that the structures are single-domain with moments that can be controlled to point either in-plane or out-of-plane. The ability of IL to pattern these large densities over large areas has the potential to provide a relatively inexpensive way to increase the density of magnetic storage media.

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